A C-BAND ALL FERRITE INTEGRATED WIDEBAND HIGH POWER GaAs AVALANCHE DIODE AMPLIFIER*

Wei C. Tsai and Chong W. Lee
Raytheon Company
Micro State-Special Microwave Devices Operation
Waltham, Massachusetts 02154

Abstract

A C-band 4-stage, 20 dB gain, 3-watt 25% bandwidth all ferrite substrate integrated GaAs avalanche diode amplifier is developed. The design procedure, as well as the amplifier performance including amplifier phase characteristics, is described. A power combining circuit which increases the output power capability by a factor of two is included in the output stage.

Design Procedure

High power GaAs avalanche diode amplifiers fabricated in alumina substrate microstrip have been reported previously.[1] The avalanche diode amplifier to be described here is constructed in ferrite substrate microstrip. It has a 20 dB gain over a 25% bandwidth centered at 5.4 GHz with a power output of 3 watts. The ferrite substrate construction eliminates the necessity of embedding the ferrite circulator puck into the dielectric MIC substrate. The amplifier chain with four cascaded amplifier stages and two isolation stages is shown in FIG. 1. The output stage has two diodes with a power combining circuit. The microstrip substrates are made of Trans Tech G1010 YIG material 40 mils in thickness with a relative dielectric constant of 15 and saturation magnetization of 1000 gauss.

Gain, bandwidth, and the output power of the amplifier depend on the avalanche diode characteristics such as the negative resistance, the diode Q and the diode power generating capability. The choice of the engineering design as shown in FIG. 1 regarding the number of stages required, the gain distribution and the diode power requirement must be based on a good knowledge of diode characteristics. Therefore, the first step in amplifier design is the diode characterization.

A large number of candidate diodes with various junction capacitance and breakdown voltage were first evaluated for their power generating capability in an oscillator cavity, and then their stable small signal impedance characteristics in a 50-ohm microstrip line were measured by a network analyzer. The measured small signal impedance data were then plotted on the Smith charts. It can be shown that the magnitude of diode Q can be calculated from the Smith chart plot by using the following equations.

$$Q = \left|\frac{X_o}{2R_D}\right| + \left|\frac{\Delta X}{2\delta R_D}\right| \qquad (1)$$

or

$$Q = \left|\frac{B_o}{2G_D}\right| + \left|\frac{\Delta B}{2\delta G_D}\right| \qquad (2)$$

where $\delta = (f_h - f_\ell)/f_o$ is the frequency deviation

ΔX and ΔB are the diode reactance and susceptance change from low band edge to high band edge

X_o and B_o are the diode reactance and susceptance at desired center frequency f_o

R_D and G_D are the diode resistance and conductance

Eq. (1) applies when the diode characteristics can be approximated by a constant resistance locus on the Smith chart and Eq. (2) applies when the characteristics can be approximated by a constant conductance locus.

It was found that the diode impedance characteristics are affected by their breakdown voltage, bias current density, and junction capacitance. Low breakdown voltage, high bias current density, and low junction capacitance force the diode impedance characteristics shift upward in frequency. From the trend of diode impedance variation with breakdown voltage, junction capacitance, and bias current density, the optimum diode design which gives the highest negative resistance and lowest diode Q in the desired frequency range was determined. A typical diode impedance characteristic is shown in FIG. 2. The diode negative resistance in the desired frequency band (4.7 to 6.1 GHz) ranges from 5 to 10 and the magnitude of diode Q ranges from 7.5 to 9. The Q of the diode limits the maximum achievable gain per stage for a given bandwidth.[2,3] The diode power requirement at a given stage gain and gain compression is determined by the "power added"[4,5] concept. By knowing the above factors, the amplifier system as shown in FIG. 1 was designed. The maximum diode Q and the minimum diode power requirements for each stage are also shown in FIG. 1.

Once the diode characterization was completed, the amplifier impedance matching network was designed for a given diode characteristic. The broadbanding technique which was described by Getsinger[3] was employed in designing a triple tuned gain response amplifier. The calculated gain

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response based on an ideal circulator, as well as the measured gain response of a single stage amplifier, is shown in FIG. 3. Note that the measured gain ripples are higher than the calculated values. This phenomena is believed to be due to the non-idealized circulator having a VSWR other than unity presented to the amplifier circuit. The single stage phase response was measured and plotted in FIG. 4. The phase linearity of the single stage amplifier is quite good except at the band edges. The phase tracking between amplifiers is expected to be good because the total phase delay is mainly determined by the total signal path through the amplifier which is accurately determined by the photographic etching method.

The gain response of the first half amplifier which includes the input isolator and two cascaded amplifier stage is shown in FIG. 5. The small signal gain ranges from 13 to 18 dB. The gain at 30 mW power input ranges from 11 to 12 dB, corresponding to the engineering design of 11.2 dB as shown in FIG. 1.

In the course of cascaded amplifier integration, some interactions between amplifier stages were observed. There are three main causes for these interactions: the dc magnetic fringing field which changes the microstrip characteristic of the adjacent stages; the RF radiation energy which couples the signal back and forth; and the finite circulator common arm isolation which creates a feed back loop from the output port to the input port of each amplifier stage. The first cause can be minimized by confining the magnetic bias field to the circulator circuit using a closed magnetic circuit. The second cause can be minimized by the physical separation of the circuit elements in the MIC layout. The third cause can be minimized by improving the common impedance match or decreasing the gain per stage.

In conclusion, a low cost, compact, wide-band, and high power avalanche diode amplifier can be integrated in an all ferrite microstrip circuit. The phase response of the integrated amplifier looks promising for many phased array applications.

References

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5. J. J. Sie and W. J. Crowe, "A One Watt CW Avalanche Diode Source or Power Amplifier," 1969 International Microwave Symposium Digest, pp 266-272.

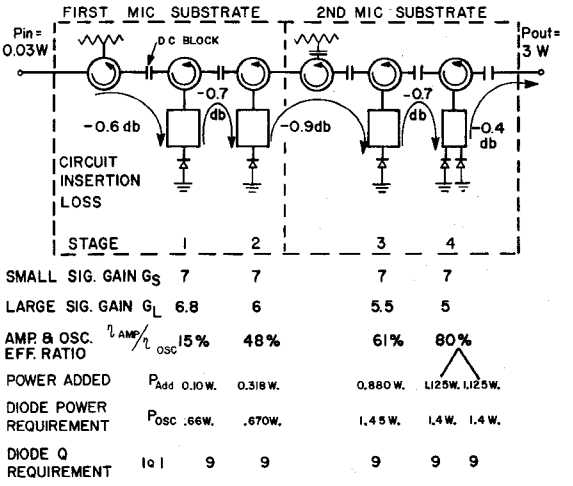

FIG. 1 THE AMPLIFIER SYSTEM EINGINEERING PLANNING

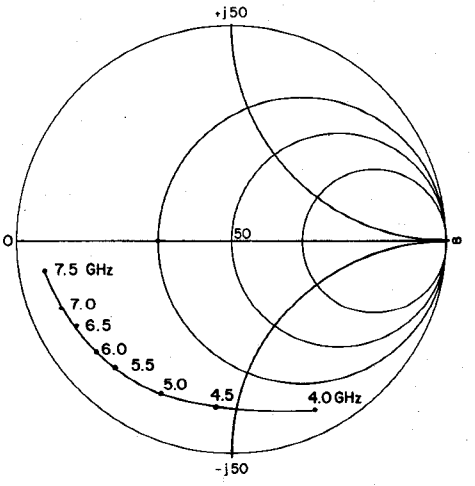

FIG. 2 THE DIODE IMPEDANCE CHARACTERISTICS

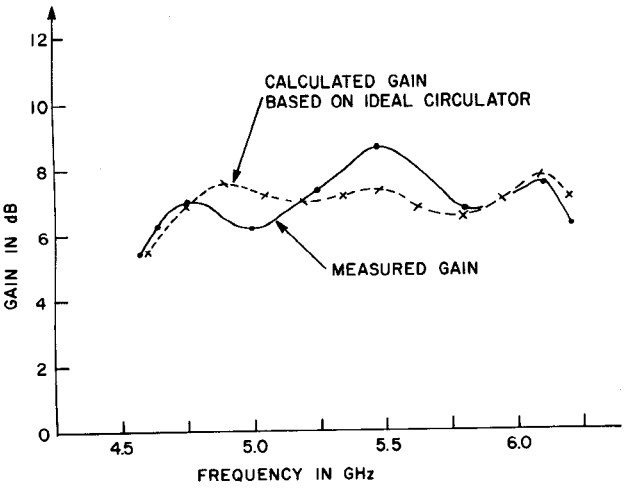

FIG. 3 THE CALCULATED AND MEASURED SINGLE STAGE GAIN RESPONSE

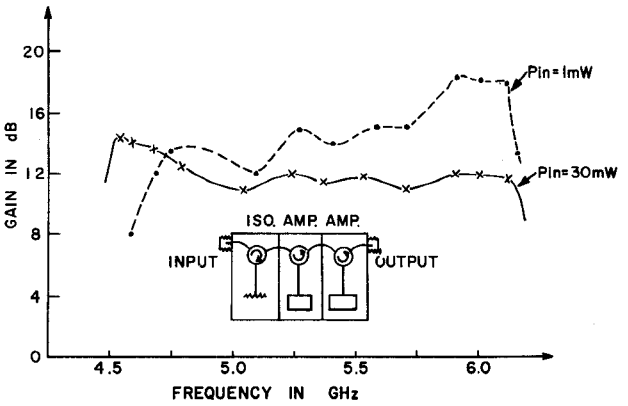

FIG. 5 THE GAIN RESPONSE OF TWO-STAGE CASCADED AMPLIFIER

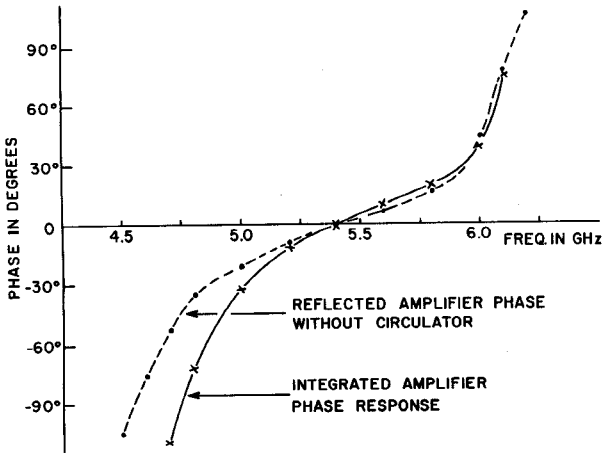

FIG. 4 THE PHASE RESPONSE OF A SINGLE STAGE AMPLIFIER